

APPLICATION FOR PATENT

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Title: NOVEL FLASH MEMORY ARRANGEMENT

5 **FIELD OF THE INVENTION**

The present invention relates to a novel flash memory arrangement, which enables executable code to be read directly from the flash memory, without requiring external memory components.

10 **BACKGROUND OF THE INVENTION**

Flash memory arrangements have many different uses, including data storage for portable devices or other devices in which storage size, weight and/or power consumption is a factor. As shown with regard to background art Figure 1, a typical flash memory arrangement 10 features a port 12 for accessing data, including both reading and writing data. The data itself is stored in a flash memory 14, which is accessible by a CPU 16 through port 12. CPU 16 is able to read and write data through port 12, by communicating with an internal processor 18. CPU 16 sends the appropriate commands to read or write data from a particular address through a bus 17. Reading and writing such data may be typically accomplished according to protocols which are known in the art, with one exception: executable code.

Executable code is actually a series of instructions which are executed by a data processor, such as CPU 16. Such executable code is required for

running software programs, and for “booting” the computational device which contains CPU 16 and flash memory arrangement 10. Typical “boot” operations include initialization of the hardware components of the computational device and also loading of required software program(s). Therefore, the ability to

5 execute instructions for booting a computational device is a clear advantage for memory components such as flash memory arrangement 10, particularly in hardware implementations in which flash memory arrangement 10 is intended to substitute for other, heavier or otherwise less suitable memory storage components, such as a magnetic medium hard disk for example.

10 Unfortunately, certain types of flash memory do not permit the direct execution of code from the memory, or “execution in place” of the code. For example, NAND flash does not permit such direct execution of code. Instead, as shown with regard to Figure 1, the code must be loaded by CPU 16 from flash memory arrangement 10 to a RAM (random access memory) 22

15 according to code which is present in an EPROM 24. Other types of memory which may be used are ROM and Nor-flash. In this example, the initial code must be loaded to EPROM 24, since flash memory 14 is a NAND-type flash memory, which requires any data to be read in blocks. Thus, initialization must occur through an additional memory component, such as EPROM 24, which is

20 not a desirable solution since it requires another component to be added to the device. Indeed, in this example, flash memory 14 is optional, since flash memory 14 cannot participate in the boot process.

Other possible solutions include using NOR-flash, which does permit execution in place, as variably-sized blocks of code may be read, but which is less desirable as it is more expensive than NAND flash. A different component than an EPROM may be used, but the requirement for any type of additional 5 memory component is less desirable as it adds to the cost and complexity of manufacture. Unfortunately, there is currently no solution to this problem.

SUMMARY OF THE INVENTION

The background art does not teach or suggest a flash memory 10 arrangement which enables flash memory devices to be used for direct execution of code even if there is a restriction on the size of blocks of data which can be read. In addition, the background art does not teach or suggest a flash memory arrangement which does not require an additional memory component in order to accomplish this goal.

15 The present invention overcomes these deficiencies of the background art, by providing a device, a method and a system for direct execution of code from a flash memory arrangement, in which a separate memory component is not required, even if a flash memory component is used which has a restriction on the size of a data block which can be read at one time. Furthermore, the 20 flash memory arrangement is optionally implemented as a “single die” chip or device, which is more efficient for manufacturing and which also results in lower costs.

According to a preferred implementation of the present invention, the flash memory arrangement features a flash memory component in direct communication with a volatile memory component, such as S-RAM or D-RAM for example. These two components are preferably arranged within a flash-based unit, and therefore communicate with a logic processor such as a CPU through the port of the flash-based unit. Thus, an additional memory component, outside the flash-based unit, is not required.

According to the present invention, there is provided a flash-based unit for providing code to be executed by an external processor, comprising: (a) a flash memory for storing the code to be executed, the flash memory being of a type such that the external processor cannot read the code to be executed directly from the flash memory; and (b) a volatile memory component for receiving at least a portion of the code to be executed, such that at least the portion of the code is executed by the external processor from the volatile memory component.

According to another embodiment of the present invention, there is provided a system for executing code from a restricted non-volatile memory, the restricted non-volatile memory being characterized in that code cannot be directly executed from the restricted non-volatile memory, the system comprising: (a) a CPU for executing the code; (b) a volatile memory component in direct communication with the restricted non-volatile memory for holding at least a portion of the code to be executed, the at least a portion of the code being transferred from the restricted non-volatile memory, such that

the CPU executes the at least a portion of the code from the volatile memory component.

According to yet another embodiment of the present invention, there is provided a system for executing code, comprising: (a) a flash-based unit for 5 storing the code to be executed, the flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot be directly executed from the flash memory and a volatile memory component for receiving a portion of the code to be executed; and (b) a processor for executing the code, the processor receiving at least the portion of the code from the volatile 10 memory component; wherein an additional memory component is not required for executing the code by the processor.

According to still another embodiment of the present invention, there is provided a method for booting a device, the device featuring a processor for executing code, the method comprising: providing a flash-based unit in the 15 device for storing the code to be executed, the flash-based unit comprising a flash memory of a restricted type, being characterized in that code cannot be directly executed from the flash memory and a volatile memory component for receiving a portion of the code to be executed; sending a busy signal to the processor; transferring the portion of the code to the volatile memory 20 component; removing the busy signal; and executing the portion of the code by the processor to boot the device.

According to another embodiment of the present invention, there is provided a flash-based unit for providing code to be executed by an external

processor, consisting essentially of: (a) a flash memory for storing the code to be executed, the flash memory being of a type such that the external processor cannot read the code to be executed directly from the flash memory; and (b) a volatile memory component for receiving at least a portion of the code to be 5 executed, such that at least the portion of the code is executed by the external processor from the volatile memory component.

Hereinafter, the terms "computer" or "computational device" refer to a combination of a particular computer hardware system and a particular 10 software operating system. Examples of such hardware systems include those with any type of suitable data processor, as well as any type of device which has a data processor of some type with an associated memory. The term "portable device" refers to any type of computer or computational device which is portable, including but not limited to, a PalmPilot™, a PilotPC™, a PDA 15 (personal data assistant) or any type of personal data player, a cellular telephone, or any other handheld device.

For the present invention, a software application could be written in substantially any suitable programming language, which could easily be selected by one of ordinary skill in the art. The programming language chosen should be compatible with the computer by which the software application is 20 executed, and in particular with the operating system of that computer.

Examples of suitable programming languages include, but are not limited to, C, C++ and Java. Furthermore, the functions of the present invention, when described as a series of steps for a method, could be implemented as a series of

software instructions for being operated by a data processor, such that the present invention could be implemented as software, firmware or hardware, or a combination thereof.

5 **BRIEF DESCRIPTION OF THE DRAWINGS**

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, wherein:

10 FIG. 1 is a schematic block diagram of a background art memory arrangement;

FIG. 2 is a schematic block diagram of an exemplary flash-based unit according to the present invention;

FIG. 3 is a flowchart of an exemplary method for operating the device of Figure 2 according to the present invention; and

15 FIG. 4 is a schematic block diagram of another implementation of an exemplary flash-based unit according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is of a device, a method and a system direct execution of code from a flash memory arrangement, in which a separate memory component is not required, even if a flash memory component is used which has a restriction on the size of a data block which can be read at one time. Furthermore, the flash memory arrangement is optionally implemented

as a “single die” chip or device, which is more efficient for manufacturing and which also results in lower costs.

According to a preferred implementation of the present invention, the flash memory arrangement features a flash memory component in direct communication with a volatile memory component, such as S-RAM or D-RAM for example. These two components are preferably arranged within a flash-based unit, and therefore communicate with a logic processor such as a CPU through the port of the flash-based unit. Thus, an additional memory component, outside the flash-based unit, is not required.

The principles and operation of a device, a system and a method according to the present invention may be better understood with reference to the drawings and the accompanying description, it being understood that these drawings are given for illustrative purposes only and are not meant to be limiting. Furthermore, although the following description centers around a NAND flash memory, it is understood that the description would be applicable to any type of non-volatile memory component with a restricted block size for reading data.

Referring now to the drawings, Figure 2 is a schematic block diagram of an illustrative, exemplary flash-based unit according to the present invention, shown as part of a system 30 for the purposes of illustration only, without any intention of being limiting. System 30 may optionally be any type of computer or computational device, as long as at least a CPU 32 (or other type of logic processor or microprocessor) and a RAM (random access memory) 34 are

present.

System 30 features a flash-based unit 36 according to the present invention, which communicates with CPU 32 and RAM 34 through a bus 38, which is a local bus. CPU 32 executes instructions, such as executable code for 5 example. CPU 32 reads these instructions from RAM 34. However, the code is stored in flash-based unit 36 as the non-volatile memory for system 30 (which may also optionally feature other types of volatile or non-volatile memory).

Flash-based unit 36 differs from the background art memory 10 arrangement in that flash-based unit 36 features a volatile memory component in direct communication with flash memory 14, shown herein as S-RAM 40 for the purposes of illustration only and without any intention of being limiting. Flash memory 14 is preferably implemented as any type of flash memory 15 component for which data can only be read in restricted block size(s) and/or which otherwise is unable to support execution of code in place. One preferred but non-limiting example of flash memory 14 is a NAND flash memory component.

Flash-based unit 36 also features a logic 42, which may optionally be a 20 CPU or other type of microprocessor, but alternatively is a plurality of logic gates, and an internal bus 37 for communication between the components of flash-based unit 36. As shown, internal bus 37 handles communication between port 12 and each of logic 42, flash memory 14 and S-RAM 40 directly. Alternatively, internal bus 37 may optionally handle communication

directly only between port 12, S-RAM 40 and logic 42. The latter component then communicates with flash memory 14 (not shown).

Flash-based unit 36 is optionally implemented as either a single-die chip or a modular component. In addition, flash-based unit 36 is also optionally 5 implemented as a BIOS, for “booting” system 30, as described for example with regard to Figure 3 below.

The operation of system 30 according to Figure 2 may optionally be performed as follows, with regard to the preferred but non-limiting example of 10 “booting” system 30 from flash-based unit 36, as shown with regard to the flowchart of Figure 3. When the “power-on” signal is received, indicating that system 30 should now “boot up”, a busy signal on bus 38 signals CPU 32 not to begin operation (stage 1). Next, a specific code (set of one or more 15 instructions) is copied automatically from flash memory 14 to S-RAM 40, without the intervention of CPU 32 (stage 2). For example, such copying of data could optionally be controlled by logic 42. S-RAM 40 is optionally very 20 small, such that the copied code is preferably only sufficient for permitting the basic initialization of system 30, and more preferably enables the remaining portion of the code to be copied to RAM 34 at a later point (see below for more details). It should be noted that at this point, copying to RAM 34 is not permitted.

Now, the busy signal goes down from bus 38 in stage 3. CPU 32 begins execution of the code in stage 4 for booting. Optionally, additional code is

copied from flash memory 14 to RAM 34 for execution as necessary, after which execution continues from RAM 34, as shown in stage 5.

According to an optional embodiment of the present invention, as shown in Figure 4, system 30 additionally features a power storage 44 for storing power. Power storage 44 may optionally be implemented as a battery, but is preferably implemented as a capacitor. In any case, power storage 44 should be independent of other sources of power to flash-based unit 36. Power storage 44 is used to provide power to flash-based unit 36, at least for a limited period of time, if flash-based unit 36 suddenly stops receiving power from other source(s).

Logic 42 preferably senses when flash-based unit 36 suddenly stops receiving power from other source(s). Next, logic 42 causes power to be drawn from power storage 44. More preferably, power storage 44 provides only a very limited amount of power, as for a capacitor for example. Most preferably, power storage 44 only provides sufficient power to enable the contents of S-RAM 40 to be copied to flash memory 14 and/or to another, more permanent memory.

It will be appreciated that the above descriptions are intended only to serve as examples, and that many other embodiments are possible within the spirit and the scope of the present invention.